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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,290	SODERQUIST ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Sweden on 09/20/2002. It is noted, however, that applicant has not filed a certified copy of the 0202792-8 application as required by 35 U.S.C. 119(b).

Drawings

3. It is requested that replacement drawings with text labels in the boxes be provided, such that the drawings can be examined and understood without having to refer back to the specification to determine what each object is.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the detector as described in Claims 2 and 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 3 claims "the detector is arranged to detect input signals by determining input signals by determining the energy level in the signal". Nothing relating to an "energy level" is found in the specification, nor is a detector found in the specification or the drawings. Claim 7 claims vector memory that has "low granularity", but no mention of granularity is found in the specification. Claims 7 and 8

refer to a "high-resolution part" and a "low-resolution part", which are also not found in the specification.

7. It is requested that the specification be amended to show where the detailed description for Figure 5 begins, which is apparently on Page 6, Line 25.

Claim Objections

8. In Claim 1, Line 5, it is believed that the word "event" should read "events". Appropriate correction or clarification is required.

9. In Claim 1, it is not clear exactly what is meant by "the instruction memory is arranged to include time performance constraints and event". For the remainder of this office action, it has been interpreted to mean that the instruction memory can contain instructions that need to be processed in real-time with deadlines (time performance constraints) and instructions that are run as a reaction to an event (events). Appropriate clarification of these terms is required.

10. In Claim 5, it is stated that in line 2 that "... as a consequence of the previous event". However, there has been no previous event introduced in Claim 1, and thus the previous event lacks antecedent basis. It is believed that the applicant intended for the claim to read "a previous event" and has been interpreted as such for the remainder of the office action. Appropriate correction is required.

11. Claim 9 ends in two periods, and should only end in one. Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 3, 7, 8, and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 3 recites the limitation "energy level" in line 2. There is insufficient antecedent basis for this limitation in the claim, as the term has not been found in the specification. It has been assumed throughout this office action to mean whether or not the signal is a "0" or a "1", i.e. its binary value.

15. Claim 7 recites the limitation "granularity" and "low granularity" in line 2. There is insufficient antecedent basis for this limitation in the claim, as these terms are not found in the specification. Granularity is believed to refer to the readable size of the memory, although the adjective "low" is not specific enough to understand the true meaning due to the lack of definition in the specification. Therefore, the term "low granularity" will be assumed to refer to any standard and well-known memory readable size.

16. Claims 7, 8, and 9 recite the limitations "high" or "low" resolution. There is insufficient antecedent basis for these limitations in the claims, as these terms are not found in the specification. Therefore, resolution is believed to refer to the amount of time required for the instruction to run under constraints, where a high-resolution part is in some way more precise or requires quicker execution than a low-resolution part, and is assumed as such for the remainder of the office action.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Knapp et al. (USPN 5,826,072, herein Knapp).

19. As per Claim 1, Knapp teaches: A digital signal processor comprising:

an instruction memory (Column 5, Lines 56-58), a central arithmetic unit (Column 6, Lines 10-12, the ALU), a register (Column 5, Lines 61-62), a controller (Column 5, Lines 62-63, the interrupt control logic), and input/output devices (Column 6, Line 1);

characterized in that

the instruction memory is arranged to include time performance constraints (Column 2, Lines 25-27) and event (Column 5, Line 64 – Column 6, Line 5);

the controller is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit (Column 5, Line 64 – Column 6, Line 5. For the remainder of this office action, it is assumed that the "event control unit" not only executes in a reaction to an event, but also is also the part of the processor that executes and/or schedules all instructions. This assumption is made by viewing Page 2, Lines 29-32 of the specification, where it appears that the event control unit is also responsible for executing or scheduling the "time performance constraints", in addition to the events. When the event (the interrupt in this case) is activated, it is run, and afterwards, the original instructions can resume running. By having to return to where the program was interrupted, it is clear that Knapp halts execution of the instruction flow during the interrupt);

the event control unit is arranged to recognize an event and to control processing to be carried out as a consequence of the event (Column 5, Line 64 – Column 6, Line 9. Also see Column 7, Lines 18-32) while fulfilling the time performance constraints (Column 6, Lines 3-5, it returns to the normal instruction flow (the time performance constraint instructions) when the event is finished) and the controller is arranged to resume processing when advised by the event control unit (Column 6, Lines 3-5).

20. As per Claim 2, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event is recognized in a detector (Column 5, Lines 61-63. The

interrupt control logic functions as a detector, as it receives interrupt request signals, and as shown in Column 6, Lines 2-5, responds to the event as a consequence of those signals being detected) and introduced as a level transition to the event control unit (Column 5, Line 64 – Column 6, Line 9, where the event control unit takes control and feeds the interrupt address to the processor).

21. As per Claim 3, Knapp teaches: A digital signal processor in accordance with claim 2, wherein the detector is arranged to detect input signals by determining the energy level in the signal (inherent that the control logic would be able to differentiate between a logic "0" and "1" on a signal line).

22. As per Claim 4, Knapp teaches: A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of the previous event (Column 10, Lines 11-14, where there needs to be an explicit signal (or instruction) to end an interrupt).

23. As per Claim 5, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of the previous event (Column 10, Lines 11-14, where there needs to be an explicit signal (or instruction) to end an interrupt).

24. As per Claim 6, Knapp teaches: A digital signal processor in accordance with claim 1, including a signal memory arranged to store and extract data under control of the event control unit (Column 6, Lines 26-29, data memory 90).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp, in view of Moorer (USPN 4,497,023), and further in view of Morrison et al. (USPN 4,847,755, herein Morrison).

27. As per Claim 7, Knapp teaches: A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory (Column 12, Lines 65-66 show that the memory can be a "vector memory") with low granularity (based on the assumed definition of what is meant by granularity, it is inherent that Knapp would have used a standard sized granularity in his invention), but fails to teach:

and where the granularity determines a split between a high-resolution part and a low-resolution part of the time performance constraints.

Moorer teaches two different types of time performance constraints (or deadlines), a timed and untimed, where an untimed (high-resolution) instruction is

executed as soon as possible, and a timed instruction (low-resolution) is executed as soon as possible, in the needed order of execution (Column 4, Lines 60-64). Morrison teaches a "time driven decentralized control", derived from the "firing time" of the instruction, based in at least part on the granularity of the system (Column 4, Lines 36-65). The advantage of Moorers system of using timed and untimed instructions is being able to prioritize which instructions need to execute first to maintain the time constraints of the system. Given that advantage, one of ordinary skill in the art at the time the invention was made would have recognized the value of separating the time constraints into timed and untimed (or high and low resolution) parts, to ensure deadlines don't get passed. The advantage of Morrisons invention is more efficient scheduling, which means better performance. One of ordinary skill in the art at the time the invention was made would have therefore used Morrisons invention to more efficiently schedule resources and increase performance by utilizing, among other things, memory granularity.

28. As per Claim 8, Knapp teaches: A digital signal processor in accordance with claim 7, wherein the event control unit is arranged to process the low-resolution part (as discussed in the Claim 1 rejection, the event control unit is the general execution/scheduling unit in the system, and would thus process the low-resolution part when it got to the front of the queue).

29. As per Claim 9, Knapp teaches: A digital signal processor in accordance with claim 7, wherein the high-resolution part is processed during memory access to the signal memory by delaying the access to the signal memory a period of time corresponding to the high-resolution part (As discussed in the Claim 1 rejection, it is clear that Knapp only executes one instruction at a time per event control unit. As the high-resolution (untimed) instructions have to be executed immediately, they would require that any other instructions to be delayed while the instruction finished, thus delaying access to the memory until the high-resolution part is finished).

30. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp, in view of Patterson et al. (herein Patterson).

31. As per Claim 10, Knapp teaches A digital signal processor in accordance with claim 1, but fails to teach: including two or more event control units arranged to work independently from each other.

However, Patterson teaches the idea of making a processor superscalar. A superscalar processor can execute multiple instructions at the same time, as long as they remain independent of each other (Pages 278-279). As assumed in the Claim 1 rejection, an "event control unit" appears to be a general execution unit, as it appears to work on all kinds of instructions in the processor. As shown in Patterson, and as one of ordinary skill in the art would recognize, the advantage of parallel processing is to increase performance by decreasing the cycles per instruction of the processor (Page 278). Given this advantage, it would have been obvious to one of ordinary skill in the art

to apply the knowledge of superscalar processors to Knapps invention, and apply the same mechanic to the event control units, to allow for multiple units to execute simultaneously and independently for increased overall performance.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

33. LoGalbo et al. (USPN 5,220,676) teaches a high-resolution and a low-resolution clock used to synchronize a system.

34. Polan et al. (USPN 6,892,167) teaches a high and low resolution clock used for generating precise time stamps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
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